WHAT IS CLAIMED IS:

1. A deep trench structure of semiconductor device, said semiconductor device having a plurality of active areas, said deep trench structure characterized in that said deep trench communicates with two different active areas.
2. The structure as claimed in Claim 1, wherein the cross section of said deep trench communicates with two different active areas.
3. The structure as claimed in Claim 2, wherein said two different active areas communicated by said deep trench are respectively connected with two adjacent bit lines.
4. A semiconductor memory device comprising:
   a plurality of bit lines;
   a plurality of gates crossing with said bit lines;
   a plurality of active areas, each of which is connected to one of said bit lines;
   a plurality of deep trenches, at least one of which communicates with two different active areas.
5. The device as claimed in Claim 4, wherein the cross section of said deep trench communicates with two different active areas.
6. The device as claimed in Claim 5, wherein said two different active areas communicated by said deep trench are respectively connected with two adjacent bit lines.